AMENDMENTS TO THE CLAIMS

Listing of claims:

The following is a complete, marked up listing of revised claims with a status identifier in parentheses, underlined text indicating insertions, and strikethrough and/or double-bracketed text indicating deletions.

1-18. (Cancelled)

19. (Previously Presented) A semiconductor integrated circuit device, comprising:

a power terminal receiving a high voltage higher than a power supply voltage of the device;

a first MOS transistor coupled between the power terminal and a first internal node, the first internal node coupled to a row decoder and driver block of [[the]]a memory device, and the row decoder and driver block selectively drives word lines of the memory device in response to [[the]]a row address signal;

a second MOS transistor coupled between the power terminal and a second internal node,

a third MOS transistor, having a relatively thin gate insulation layer, coupled between the first internal node and a third internal node;

a fourth MOS transistor, having a relatively thin gate insulation layer, coupled between the second internal node and a fourth internal node;

a fifth MOS transistor coupled between the third internal node and a ground voltage, the fifth MOS transistor controlled by a first input signal, and the first input signal includes [[a]]the row address signal and a block selecting signal from [[a]]the memory device; and

a sixth MOS transistor coupled between the fourth internal node and the ground voltage, the sixth MOS transistor controlled by an inverted version of the first input signal.

20. (Previously Presented) The device of claim 19, wherein

the first MOS transistor and the second MOS transistor each have a relatively thick gate insulation layer, and

the fifth MOS transistor and sixth MOS transistor each have a relatively thin gate insulation layer.

21. (Previously Presented) The device of claim 19, wherein

the power supply voltage is an external power supply voltage for the device or an internal power supply voltage of the device.

22. (Original) The device of claim 19, wherein the first MOS transistor is controlled by a voltage of the second internal node, and the second MOS transistor is controlled by a voltage of the first internal node.

23. (Previously Presented) The device of claim 19, wherein gates of the third and fourth MOS transistors are coupled to a low voltage that is lower than the high voltage.

24. (Previously Presented) The device of claim 23, wherein

the power supply voltage is an external power supply voltage for the device or an internal power supply voltage of the device, and

the low voltage is one of the power supply voltage, a voltage lower than the power supply voltage, and a voltage between the power supply voltage and the high voltage.

25. (Cancelled)

26. (Previously Presented) The device of claim 19, wherein the first input signal and its inverted version are selectable to have one of a high level of a low voltage and a low level of the ground voltage.

27-28. (Cancelled)

29. (Previously Presented) The device of claim 19, wherein

the row decoder and driver block includes a plurality of row decoder and driver circuits, each row decoder and driver circuit corresponding to a given word line, and

each row decoder and driver circuit further including:

a seventh MOS transistor having a source coupled to the high voltage, a drain coupled to a fifth internal node, and a gate connected to receive a second input signal; and

eighth and ninth MOS transistors serially coupled between the fifth internal node and the ground voltage,

wherein each of the seventh and eighth MOS transistors has a relatively thick gate insulation layer, and the ninth MOS transistor has a relatively thin gate insulation layer; and

wherein the eighth MOS transistor is controlled by a voltage of the first internal node.

30. (Previously Presented) The device of claim 29, further comprising:

an inverter coupled to the corresponding fifth internal node, wherein the inverter drives the corresponding word line of each of the row and driver circuits.

31. (Previously Presented) The device of claim 30, wherein the inverter includes PMOS and NMOS transistors, each PMOS or NMOS transistor operating at another voltage higher than the power supply voltage and having a relatively thick gate insulation layer.

32-37. (Cancelled).